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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/876,522	06/07/2001	Charles Cohn	COHN 9	9236

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EXAMINER	
MUTSCHLER, BRIAN L	
ART UNIT	**PAPER NUMBER**
1753	

DATE MAILED: 05/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No.	Applicant(s)	
	09/876,522	COHN, CHARLES	
	Examiner	Art Unit	
	Brian L. Mutschler	1753	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 24 April 2003 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☐ The period for reply expires _____months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.
2. ☐ The proposed amendment(s) will not be entered because:
   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ they raise the issue of new matter (see Note below);
   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: _____.
3. ☒ Applicant's reply has overcome the following rejection(s): See Continuation Sheet.
4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *See Continuation Sheet*.
6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.
7. ☒ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: *1-14 and 21-24*.

   Claim(s) withdrawn from consideration: _____.
8. ☐ The proposed drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.
9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.
10. ☐ Other: _____

Continuation of 3. Applicant's reply has overcome the following rejection(s): The rejection of claims 1-14 and 21-24 under 35 U.S.C. 112, second paragraph, has been overcome by Applicant's amendment to provide antecedent basis for the limitations in the claims.

Continuation of 5. does NOT place the application in condition for allowance because: It is the Examiner's position that the interconnect disclosed by Lim comprises the prescribed features 97 and 99, interconnects 102 and 104 and the material shown to be contained within the holes 101a and 101b. According to the disclosure corresponding to Figure 6B, the copper material contained within the holes 101a and 101b is deposited in the plating step of forming prescribed features 97 and 99. It is also the Examiner's position that the copper material contained within the holes 101a and 101b is electrically and physically connected to the features identified by references signs 97 and 99 for two reasons. First, the device would not function in its intended use as a printed circuit board unless the features formed a circuit. Second, the connectivity of the material within the holes 101a and 101b is further evidenced by the other embodiments disclsoed by Lim. In Figure 3E, reference sign 62 is used to identify the material within the opening 60. Interconnect 62 is further covered by additional metal layer 66, which is shown to be connected to the material 62 within the hole 60 and the "isolated" features shown separated from the material in and above the hole. Both the material connected to interconnect 62 and the "isolated" material are identified by reference sign 66, which is disclosed in the specification as "circuitry" (par. [0023]). The term circuitry is used to define an electrical circuit, which as is well known in the art, means a connected electrical path. Further evidence for the Examiner's position can be found in Figure 5 and paragraph [0026], which disclose the printed circuit boards formed by the method as having "three core layers (80, 82 and 84) and four circuitrized metallic layers (86, 88, 90, and 92), and a solid metallic interconnect which connects metallic layers 88, 90 and 92 as shown in Fig. 5." As seen in Figure 5, circuitrized metallic layers 88, 90 and 92 are shown to be isolated in the cross sectional representation, yet the solid metallic interconnect "connects metallic layers 88, 90 and 92". In light of the evidence provided by Lim, it is the Examiner's position that the material within the holes 101a and 101b is in electrical contact with the labeled features 97 and 99, and therefore, Lim teaches all of the limitations recited in the instant claims.

Regarding Applicant's argument on page 10 of the response, wherein Applicant states, "the portion of the interconnect relied on by the Examiner does not meet the elements of the interconnect as recited in the independent claims". Applicant bases this argument on the reasoning that the instant claim recites, "'an' inteconnect is formed through the via" and apparently does not agree that Lim shows an interconnect being formed through the via. As can be clearly seen between Figures 6A and 6B of Lim, the dielectric material begins without any holes. Holes 101a and 101b are formed in the dielectric 94, followed by a plating step to deposit features 97 and 99. As shown in Figure 6B, this deposited material not only forms the features explicitly identified by the reference signs 97 and 99, but also shows the same material to be present within and surrounding the holes 101a and 101b. Further evidence that the features 97 and 99 are in fact connected to an interconnect is shown in Figure 5 and its corresponding description in paragraph [0026], which states the metallic layers are connected by a metallic interconnect.

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